

## **AMENDMENTS TO THE CLAIMS**

This listing of claims will replace all prior versions, and listings, of claims in the application:

### **Listing of Claims:**

1           1. (Previously presented) A method for measuring alignment between a  
2 first semiconductor die and a second semiconductor die, comprising:  
3           applying a pattern of voltage signals to a two-dimensional array of  
4 conductive transmitter elements that form a transmitter array on the first  
5 semiconductor die;  
6           wherein the transmitter array on the first semiconductor die is located over  
7 a corresponding two-dimensional array of conductive receiver elements that form  
8 a receiver array on the second semiconductor die;  
9           wherein transmitter elements have a different spacing than receiver  
10 elements, whereby a two-dimensional vernier alignment structure is created when  
11 the transmitter array is located over the receiver array;  
12           wherein a voltage signal applied to a transmitter element induces a voltage  
13 signal in one or more receiver elements;  
14           amplifying voltage signals induced in receiver elements in the receiver  
15 array; and  
16           analyzing the amplified signals to determine an alignment between the  
17 first semiconductor die and the second semiconductor die.

1           2 (Canceled).

1           3. (Original) The method of claim 1,

2            wherein the transmitter array is organized as a two-dimensional  $n \times m$  grid  
3 including  $nm$  conductive elements; and  
4            wherein the receiver array includes at least three conductive elements  
5 which are not collinear.

1            4. (Original) The method of claim 1,  
2            wherein the receiver array is organized as a two-dimensional  $n \times m$  grid  
3 including  $nm$  conductive elements; and  
4            wherein the transmitter array includes at least three conductive elements  
5 which are not collinear.

1            5. (Original) The method of claim 1, wherein determining the alignment  
2 involves determining six degrees of alignment, including:  
3            an  $x$  alignment parallel to plane of the receiver array;  
4            a  $y$  alignment parallel to plane of the receiver array and normal to the  $x$   
5 axis;  
6            a  $z$  alignment normal to the plane of the receiver array;  
7            an angular alignment,  $\theta$ , about the  $z$  axis;  
8            an angular alignment,  $\Psi$ , about the  $y$  axis; and  
9            an angular alignment,  $\Phi$ , about the  $x$  axis.

1            6. (Original) The method of claim 5, wherein determining the alignment  
2 involves analyzing coupling capacitances between individual receiver elements  
3 and individual transmitter elements to determine the  $x$  alignment, the  $y$  alignment  
4 and the angular alignment,  $\theta$ .

1           7. (Original) The method of claim 6, wherein analyzing the coupling  
2 capacitances involves determining a nearest neighbor mapping between receiver  
3 elements and transmitter elements.

1           8. (Original) The method of claim 5, wherein determining the alignment  
2 involves using a mapping function generated by a three-dimensional capacitance  
3 field solver simulation to determine the z alignment, the angular alignment,  $\Psi$ , and  
4 the angular alignment,  $\Phi$ .

1           9. (Original) The method of claim 5, wherein determining the z alignment,  
2 the angular alignment,  $\Psi$ , and the angular alignment,  $\Phi$ , involves summing  
3 capacitances between individual receiver elements in the receiver array and all  
4 transmitter elements in the transmitter array, thereby effectively considering the  
5 transmitter array to be one large plate.

1           10. (Original) The method of claim 5, wherein determining the z  
2 alignment, the angular alignment,  $\Psi$ , and the angular alignment,  $\Phi$ , involves  
3 summing capacitances between individual transmitter elements in the transmitter  
4 array and all receiver elements in the receiver array, thereby effectively  
5 considering the receiver array to be one large plate.

1           11. (Original) The method of claim 1, further comprising electrically  
2 varying the pitch of the transmitter array by grouping together adjacent transmitter  
3 elements.

1           12. (Original) The method of claim 1, further comprising electrically  
2 varying the pitch of the receiver array by grouping together adjacent receiver  
3 elements.

1           13. (Original) The method of claim 1, wherein transmitter elements and  
2 receiver elements are:  
3           square;  
4           rectangular;  
5           hexagonal;  
6           triangular;  
7           oval; or  
8           round.

1           14. (Original) The method of claim 1,  
2 wherein transmitter elements are located in a metal layer of the first  
3 semiconductor die and are not covered by higher layers of metal; and  
4 wherein receiver elements are located in a metal layer of the second  
5 semiconductor die and are not covered by higher layers of metal.

1           15. (Previously presented) An apparatus that measures alignment between  
2 a first semiconductor die and a second semiconductor die, comprising:  
3           a two-dimensional array of conductive transmitter elements that form a  
4 transmitter array on the first semiconductor die;  
5           a two-dimensional array of conductive receiver elements that form a  
6 receiver array on the second semiconductor die;;  
7           wherein transmitter elements have a different spacing than receiver  
8 elements, whereby a two-dimensional vernier alignment structure is created when  
9 the transmitter array is located over the receiver array;  
10          a driving mechanism configured to apply a pattern of voltage signals to the  
11 transmitter array;

12            wherein a voltage signal applied to a transmitter element induces a voltage  
13            signal in one or more receiver elements when the transmitter array is located over  
14            the receiver array;  
15            an amplification mechanism configured to amplify voltage signals induced  
16            in receiver elements in the receiver array; and  
17            an analysis mechanism configured to analyze the amplified signals to  
18            determine an alignment between the first semiconductor die and the second  
19            semiconductor die.

1            16 (Canceled).

1            17. (Original) The apparatus of claim 15,  
2            wherein the transmitter array is organized as a two-dimensional  $n \times m$  grid  
3            including  $nm$  conductive elements; and  
4            wherein the receiver array includes at least three conductive elements  
5            which are not collinear.

1            18. (Original) The apparatus of claim 15,  
2            wherein the receiver array is organized as a two-dimensional  $n \times m$  grid  
3            including  $nm$  conductive elements; and  
4            wherein the transmitter array includes at least three conductive elements  
5            which are not collinear.

1            19. (Original) The apparatus of claim 15, wherein the driving mechanism  
2            and the analysis mechanism are configured to determine six degrees of alignment,  
3            including:  
4            an  $x$  alignment parallel to plane of the receiver array;

5 a  $y$  alignment parallel to plane of the receiver array and normal to the  $x$   
6 axis;  
7 a  $z$  alignment normal to the plane of the receiver array;  
8 an angular alignment,  $\theta$ , about the  $z$  axis;  
9 an angular alignment,  $\Psi$ , about the  $y$  axis; and  
10 an angular alignment,  $\Phi$ , about the  $x$  axis.

1 20. (Original) The apparatus of claim 19, wherein the analysis mechanism  
2 is configured to determine coupling capacitances between individual receiver  
3 elements and individual transmitter elements to determine the  $x$  alignment, the  $y$   
4 alignment and the angular alignment,  $\theta$ .

1 21. (Original) The apparatus of claim 20, wherein the analysis mechanism  
2 is configured to determine a nearest neighbor mapping between receiver elements  
3 and transmitter elements.

1 22. (Original) The apparatus of claim 19, wherein the analysis mechanism  
2 is configured to use a mapping function generated by a three-dimensional  
3 capacitance field solver simulation to determine the  $z$  alignment, the angular  
4 alignment,  $\Psi$ , and the angular alignment,  $\Phi$ .

1 23. (Original) The apparatus of claim 19, wherein the apparatus is  
2 configured to determine the  $z$  alignment, the angular alignment,  $\Psi$ , and the angular  
3 alignment,  $\Phi$ , by summing capacitances between individual receiver elements in  
4 the receiver array and all transmitter elements in the transmitter array, thereby  
5 effectively considering the transmitter array to be one large plate.

1           24. (Original) The apparatus of claim 19, wherein the apparatus is  
2 configured to determine the  $z$  alignment, the angular alignment,  $\Psi$ , and the angular  
3 alignment,  $\Phi$ , by summing capacitances between individual transmitter elements  
4 in the transmitter array and all receiver elements in the receiver array, thereby  
5 effectively considering the receiver array to be one large plate.

1           25. (Original) The apparatus of claim 15, wherein the apparatus is  
2 configured to electrically vary the pitch of the transmitter array by grouping  
3 together adjacent transmitter elements.

1           26. (Original) The apparatus of claim 15, wherein the apparatus is  
2 configured to electrically vary the pitch of the receiver array by grouping together  
3 adjacent receiver elements.

1           27. (Original) The apparatus of claim 15, wherein transmitter elements and  
2 receiver elements are:  
3           square;  
4           rectangular;  
5           hexagonal;  
6           triangular;  
7           oval; or  
8           round.

1           28. (Original) The apparatus of claim 15,  
2 wherein transmitter elements are located in a metal layer of the first  
3 semiconductor die and are not covered by higher layers of metal; and  
4 wherein receiver elements are located in a metal layer of the second  
5 semiconductor die and are not covered by higher layers of metal.